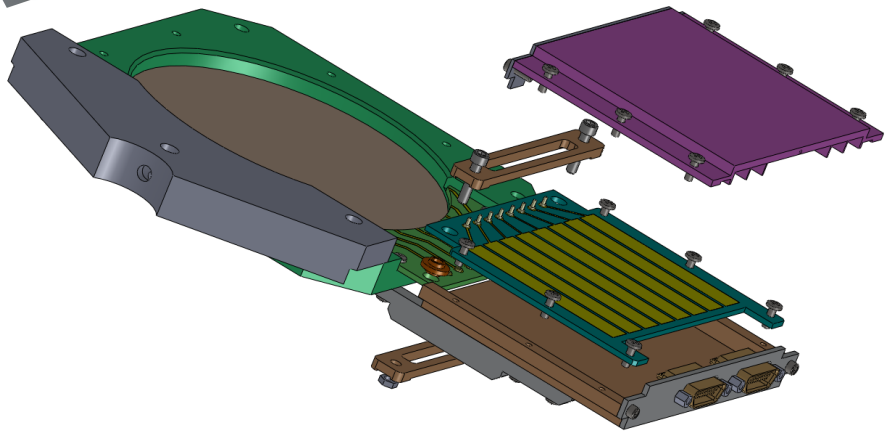
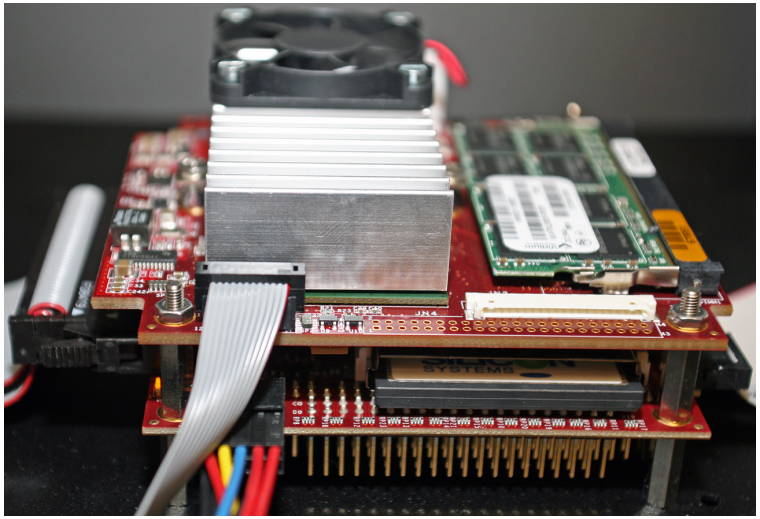
pGAPS DAQ PDR - rev.

Berkeley GAPS Group
& F. Gahbauer

October 2010





Outline for PDR

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1. Flight requirements pertaining to UCB
2. Detector Board
3. Preamp
4. Card Cages
5. Flight Computer
6. Flight software & GSE
7. Power Distribution Board
8. Harnessing
9. Power and Mass
10. Open Issues

Readout overview

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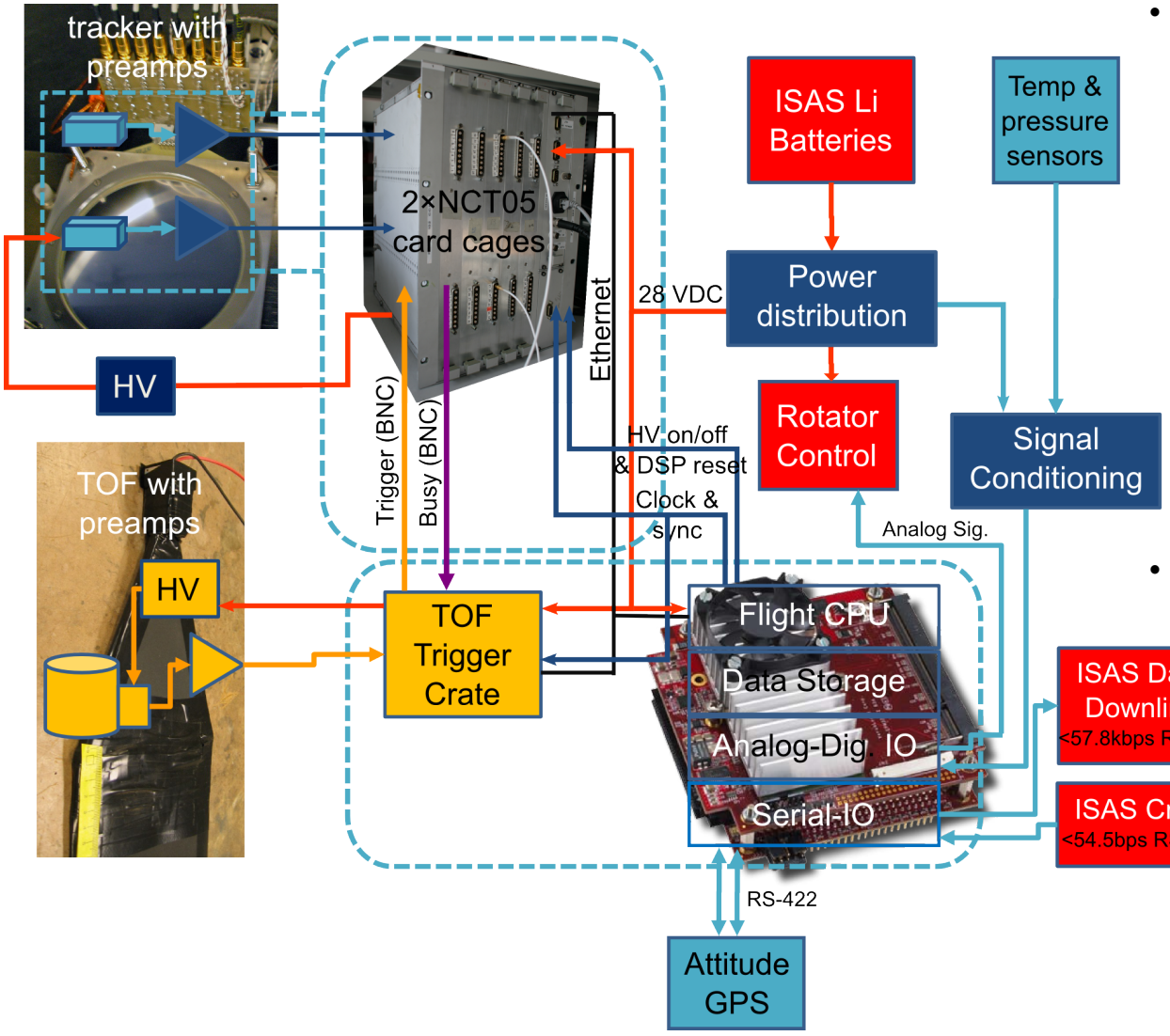

- Si(Li) tracker will be read out by two NCT 05 card cages
  - 2x72 channels:
    high gain: 0-2MeV
    low gain: 0.1-100MeV
  - sends data via Ethernet
  - external TOF trigger and self-trigger option

TOF readout by VME crate sends data via Ethernet

- Flight computer:
  - communicates via Ethernet with tracker and TOF
  - store data on compact flash cards
  - send housekeeping, portion of data to ground
  - commanding and settings

UCB Requirements - 1

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	Electrical/Power	Mechanical/Mass	Modifications
PREAMPS	Up to 10 Preamps		Up to 9 Preamps
	30mW per Preamp channel	Preamps mounted on detectors	
Energy Resolution	<3KEV (FWHM) at 60KEV		
temperature		Operating temp -35C	
Card Cages: **high gain**	80 channels 0-100KeV, 13 bits		72 channels 10KeV-2MeV, 13 bits
noise	<.1KeV (3 bits)		5 X below preamps/Det
low gain	80 channels .1-100MeV, 13 bits		72 channels 10KeV-100MeV, 13 bits
noise	<.1KeV (3 bits)		5 X below preamps/Det
	33W each	20 Kg each	
Event Rates	Data rate 6.5KB/s		
	Event Rate 30Hz		
Trigger modes			
TOF system trigger	<200Hz		100Hz, mod UCLA
Self trigger	High gain only, 30KHz in flight		5KHz maximum
UCB Vessel	76W	71 Kg	

UCB Requirements - 2

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	Electrical/Power	Mechanical/Mass	Modified
Flight CPU	20W	7Kg	
	Total data size: 100MB		
	Event Rate 50Hz		30Hz (3TOF trigger), 86Hz (2TOF trigger with veto), anyway ist must be below 100Hz
	Data Rate 500B/S		Data rate 6.5KB/s
	Data in 5h: 9MB		Total data size in 3h: 70MB
During self trigger:	High gain only, 30KHz in flight		5KHz
Harnessing		15Kg	Preamp harnessing 1.5Kg
Signal Conditioning	5W	1Kg	Housekeeping?
Power Conditioning		3Kg	Power Distribution Board: 7Kg, 2W

Detector board

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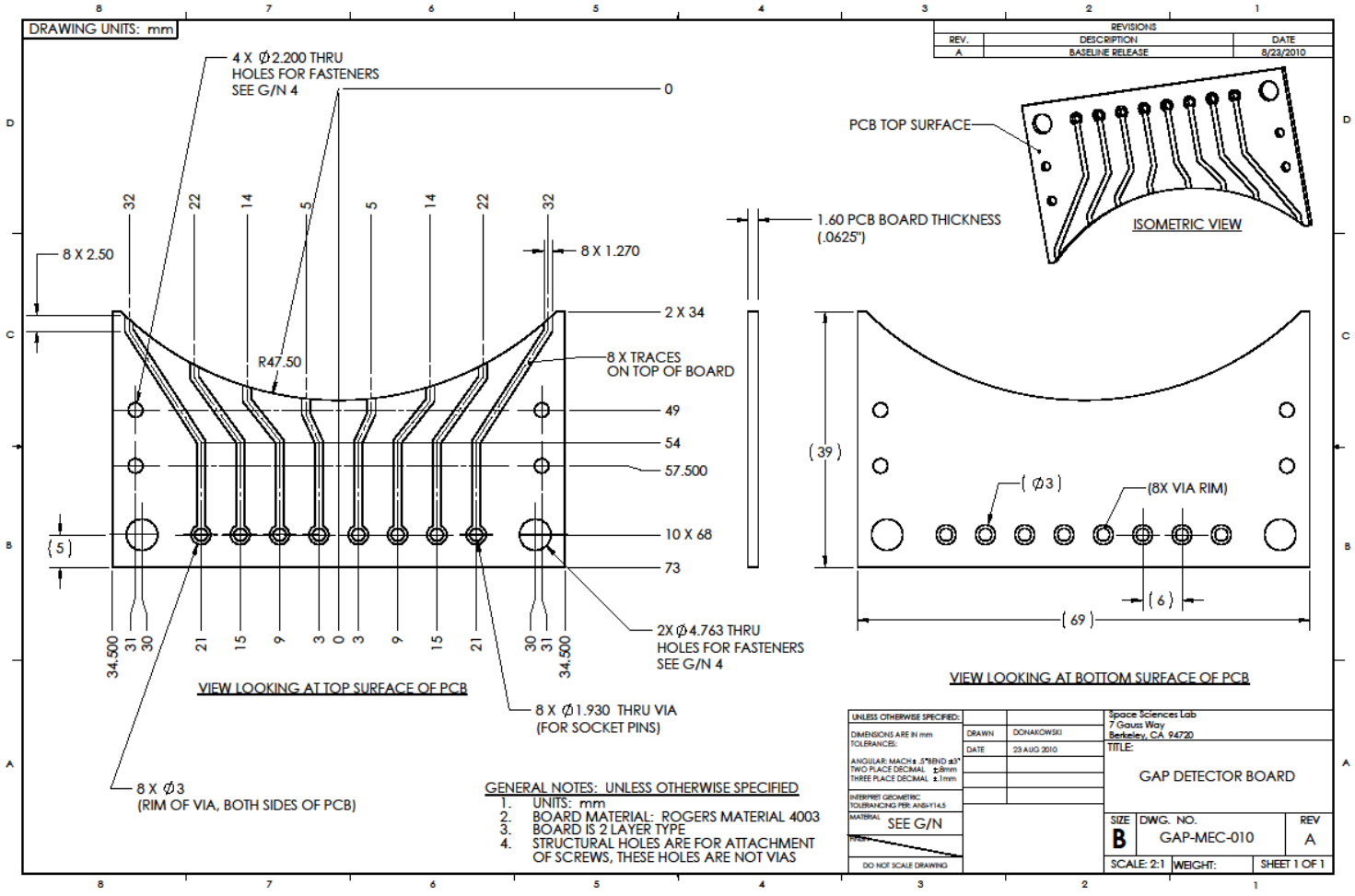

Detector board status: waiting for layout, 4 weeks to completion

Preamp and detector board

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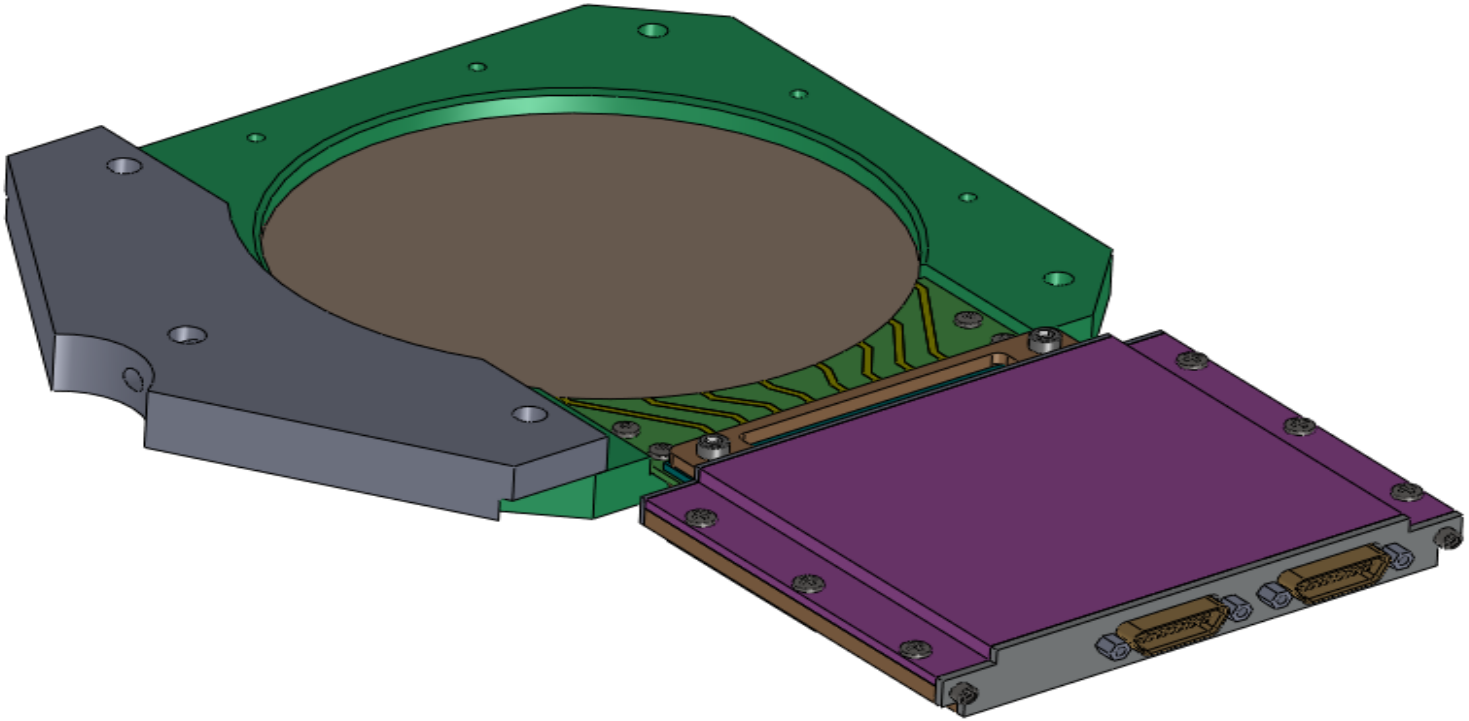

Top View: Detector, Detector Frame and Preamp

Preamp and detector board

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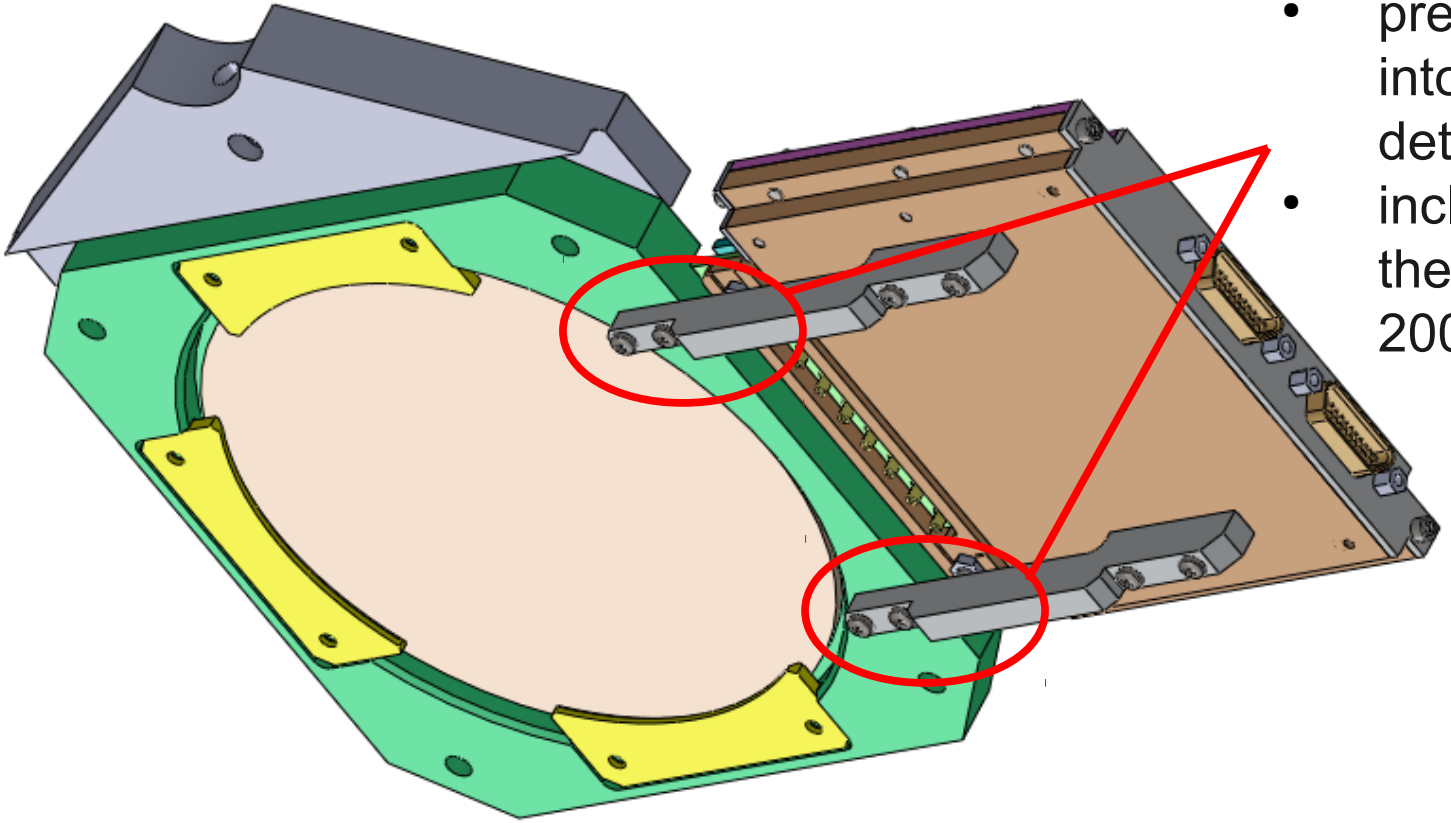
Bottom View



- preamp heat goes into frame of Si(Li) detectors
- included in the thermal design up to 200mW

Preamp and detector board

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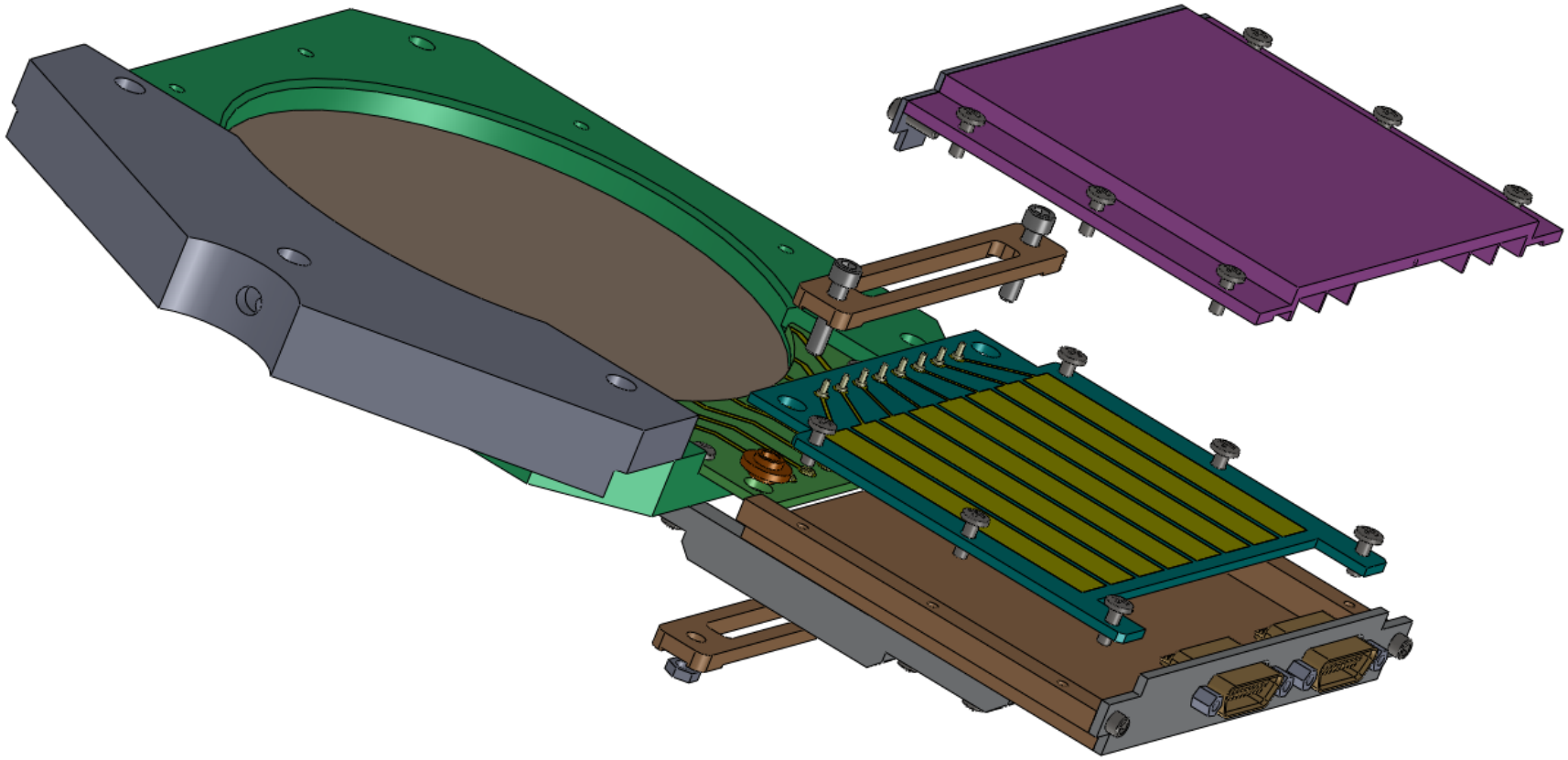
Preamp Enclosure



Preamp block diagram

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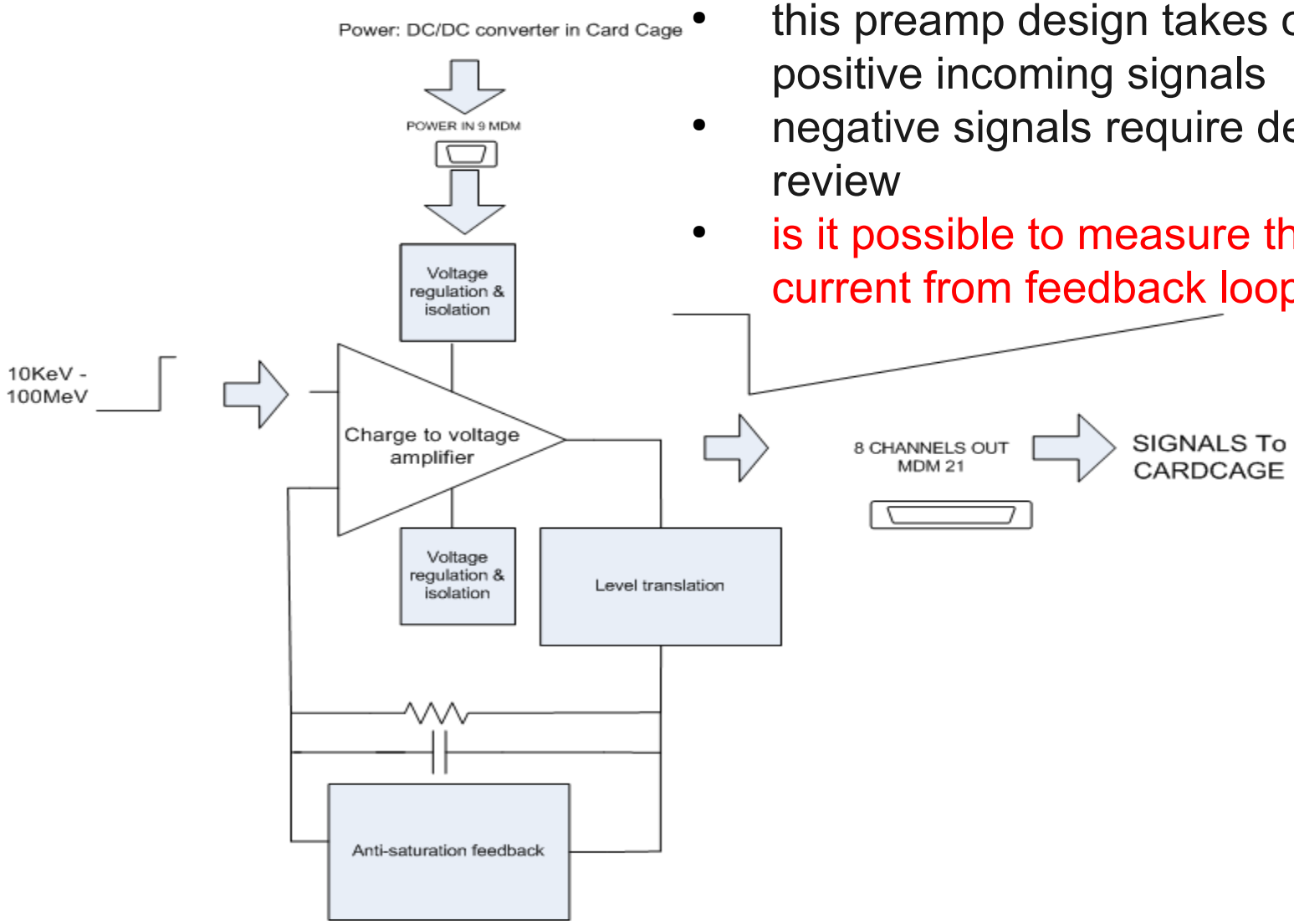

- this preamp design takes only positive incoming signals
- negative signals require design review
- is it possible to measure the dark current from feedback loop?

Preamp performance specifications

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	Preamp Performance Specification
Max # preamps	9
Power	.30W/detector
Energy Range	10KeV- 100MeV
Noise	<3KeV
temperature	-35C
mass	200g/detector
polarity	Positive input prefered
Timing (rise time)	50ns
Mounted to detector	yes

TASKS AND SCHEDULE

	Task	Completion date	comment
1	Finalize schematic, BB testing	10/18/2010	Noise and range
2	simulation	10/22/2010	
3	Order long lead parts	10/19/2010	
4	Finish mechanical drawings PCB	10/18/2010	
5	PCB layout	11/20/2010	Start 10/18
6	Finish mechanical all Drawings	10/29/2010	
7	Order parts	11/1/2010	
8	Receive mechanical parts	11/30/2010	
9	PCB fabrication	11/29/2010	Start 11/15
10	Assembly send out	12/13/2010	Start 11/29
11	Technician: assembly & cleaning	1/5/2011	
12	Board level Testing	2/3/2011	Start 1/10
13	Thermal testing	2/3/2011	
14	Box assembly & test	2/11/2011	

Could start sending boards to Columbia by end of January if nothing goes wrong.

Card cage performance specification

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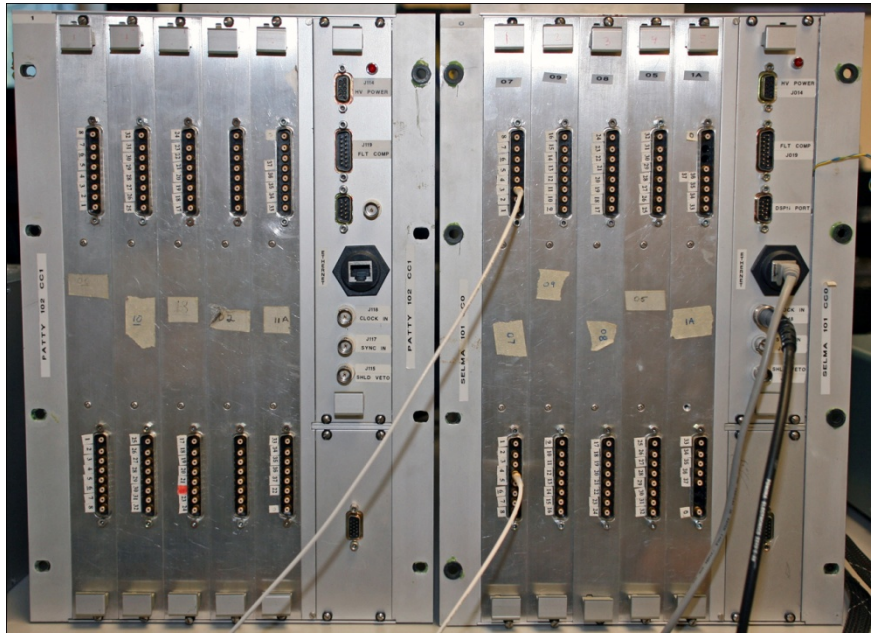
	Card Cage Performance Specification
Power	33W
Energy Range High Gain	72 channels 10KeV-2MeV, 13 bits
Noise	5 X below preamps/Det
Energy Range Low Gain	72 channels 10KeV-100MeV, 13 bits
Noise	5 X below preamps/Det
Event rate	5KHZ
mass	20Kg
Dead time	~25µs
Logic Signals	5V logic
Triggers Modes	Self trigger & TOF trigger
Housekeeping	Voltages, current, temperatures
Power for Preamps	3 x (+/- 5)
Power for HV	tbd

- UCB trigger signal has 5V
- powering/grounding of preamps/ card cages need to be studied
- 1 Si(Li) detector needs different HV



- current status of CC channels
  - out of 160 channels:
    - 12 channels channels are not connected
    - 3 channels are dead
    - 3 channels show peculiar behavior

Card cage block diagram

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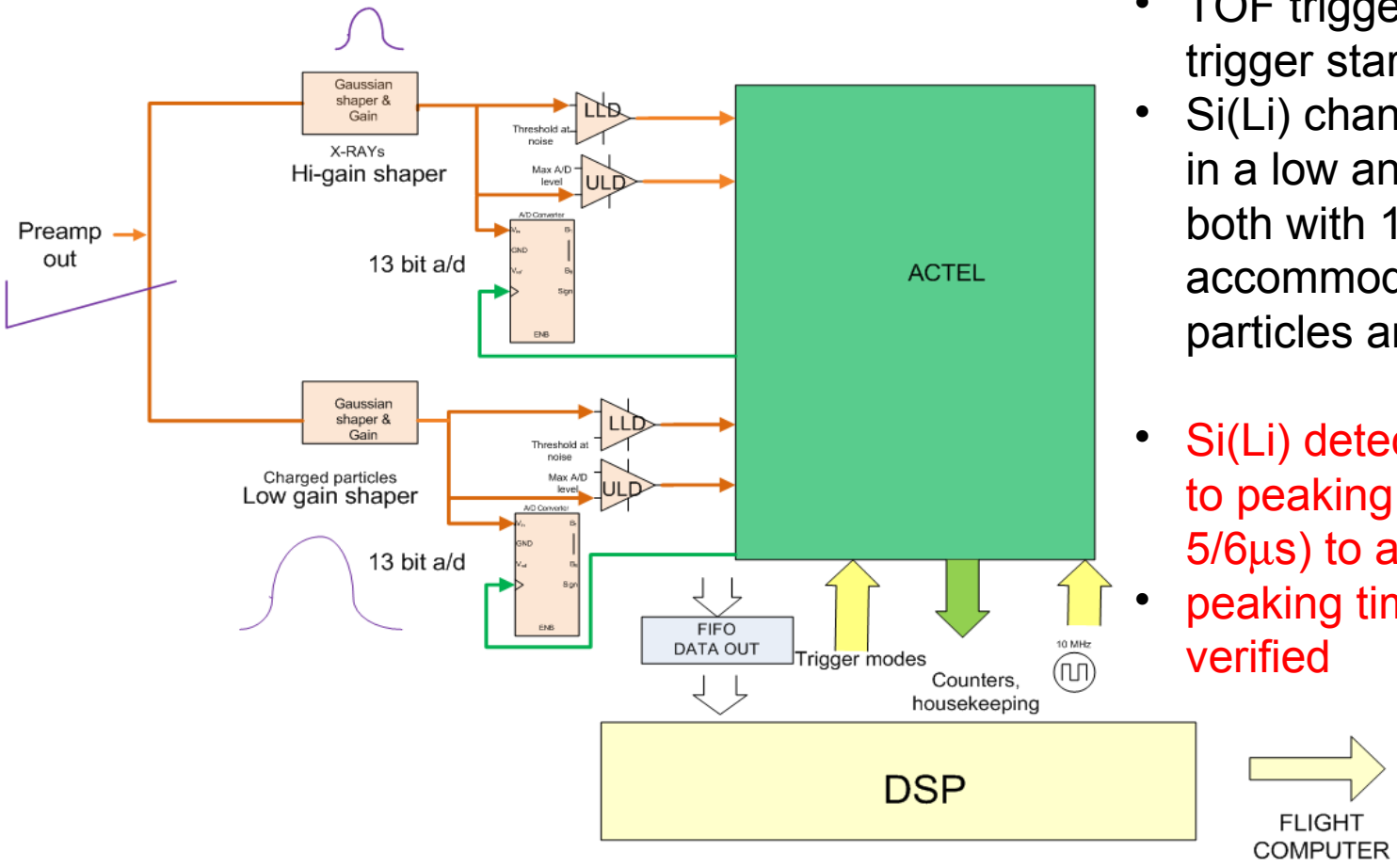

- TOF trigger or Si(Li) self-trigger starts readout
- Si(Li) channels are processed in a low and high gain branch both with 13bit ADCs to accommodate charged particles and x-rays
- Si(Li) detectors are sensitive to peaking time (optimum 3-5/6μs) to avoid degradation
- peaking time needs to be verified

Changes to card cage boards

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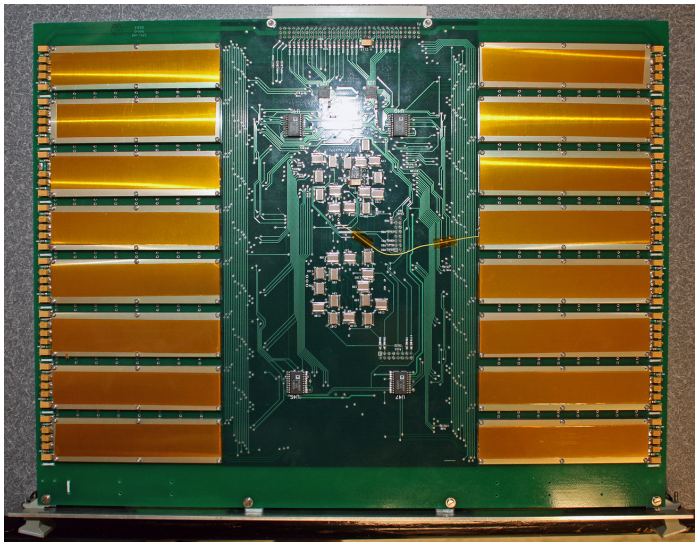
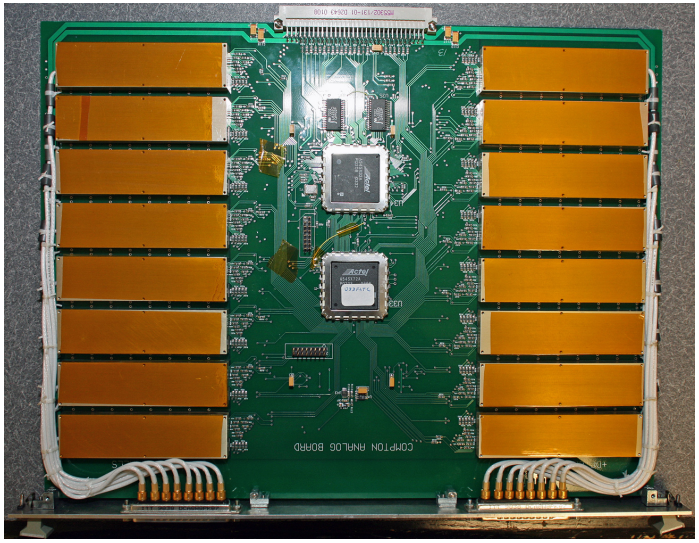
1. Change “+” channels to “-”.
2. Change gains on all channels (2 levels)
3. New wiring, each detector strip will have 2 channels with different gains.
4. New ACTEL – different triggering, different timing specifications, different inputs.
5. Instead of veto signal, TOF trigger signal.
6. New connectors.
7. DSP reprogramming
8. Institute combined busy signal
9. Change HV and Preamp Power
10. Where do the HV live?





Card cage timing

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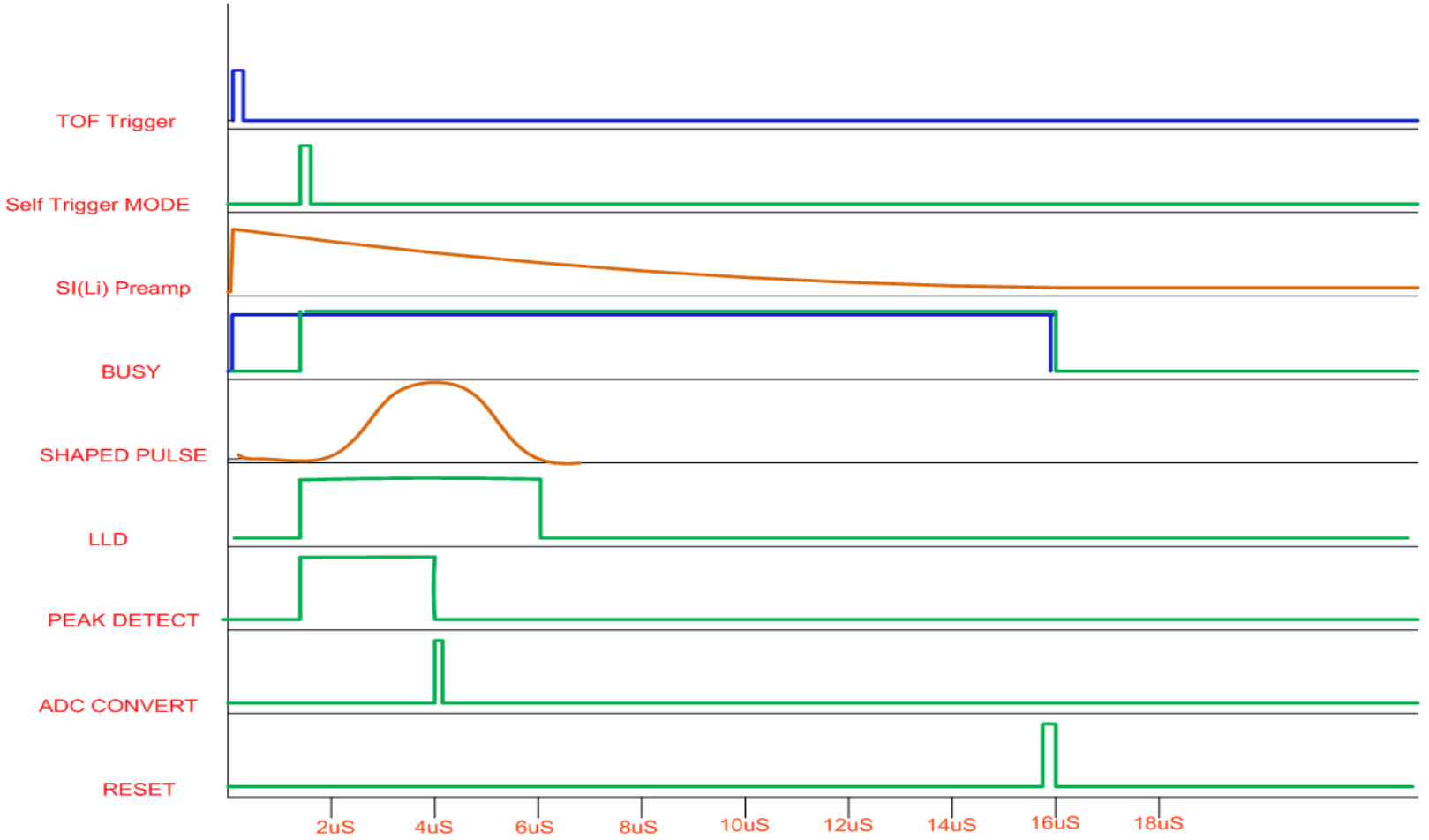

- shapers integrate everything from charge amplifier with ~4μs peaking time (verify number, What does it take to change?)
- data passed to FIFO in ~16μs

ACTEL & DSP

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- **ACTEL tasks**:
  - trigger decision for self-triggered mode: energy deposition above threshold, DSP takes decision
  - count hits above thresholds (ULD, LLD, #TOF trigger, [#self-trigger during TOF mode])
  - ACTEL controls the A/D conversion based on LLD, ULD, peak detection (LLD threshold = 2σ pedestal, ULD threshold is set to the maximum for a non-overflow A/D conversion)
  - after trigger fill FIFO with system clock (32bit/10MHz), trigger condition and high gain or low gain ADC values (each board has 8 high and 8 low gain channels)
  - BUSY is sent
  - ACTEL resets after each event
  - include UCLA in ACTEL design to make sure that the trigger is correctly understood

- **DSP tasks**:
  - check data quality
  - compressed mode: send out only non-zero ADC values
  - sends the data via Ethernet to flight computer using the UDP protocol
  - controls threshold DACs on boards via ACTELs

Card cage housekeeping data

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- Voltage and current monitors for all analog and digital supplies: +5VA, -5VA, +5VD, +12VD, and +2.5VD.
- 4 temperature monitors that can be put on sensitive or power hungry parts inside the card cages.

Card cage – Tasks and schedule

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	Task	Completion date	comment
1	Finalize changes to schematic, & BB testing	11/5/2010	
2	Order parts	11/9/2010	
3	Modify Analog boards	1/28/2011	Start 11/15/2010
4	Modify back plane	1/28/2011	
5	Order DC/DC converters preamps	11/15/2010	
6	Order DC/DC converters HV	11/15/2010	Need specification from CU
7	Filtering/shielding boxes	11/17/2010	
8	Assembly of power supply boxes	11/30/2010	
9	ACTEL changes	12/30/2010	
10	DSP programming	1/30/2011	
11	End to end Testing	2/3/2011	Started 9/2010

Flight computer

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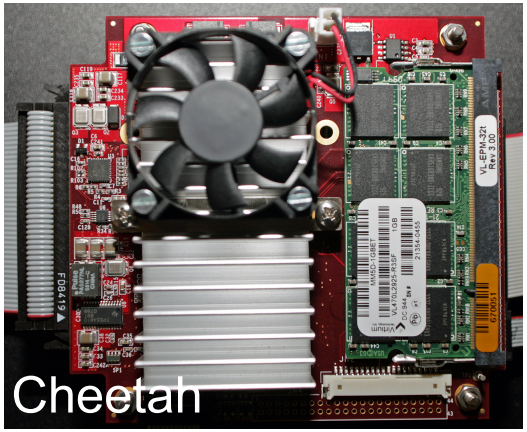
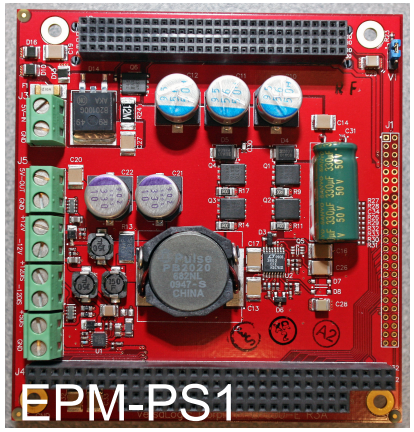
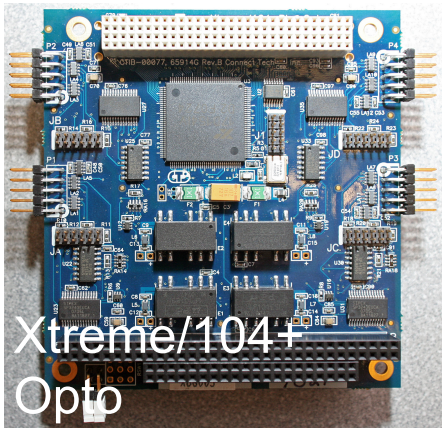

Cheetah


EPM-PS1


Xtreme/104+ Opto


DIAMOND-MM-32DX-AT32DX-AT

- PC/104(+) stack:
  - Versalogic Cheetah:
    2 boards with CPU, fan, DDR RAM and CF card slot (1.8GHz, Ethernet), 2 COM ports
  - Versalogic EPM-PS1: 50 Watt power supply
  - Xtreme/104+ Opto:
    serial communication
  - DIAMOND-MM-32DX-AT: 32 analog inputs, 4 analog outputs, 24 Digital I/O with programmable direction
  - empty module for mounting of 2rd CF card
  - clock module (Steve McBride)
- operating system: Debian Kernel, 2.6.28
- Storage: 2 compact flash cards (1GB)

Flight computer tasks

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- receive Ethernet data streams from TOF and from two UCB Card Cages (Si(Li) data) and receive housekeeping data
- write all data to disk
- send (portion of) data to ISAS telemetry via RS232C
- receive telemetry commands and execute (via digital I/O or send to TOF subsystem via Ethernet)
- control rotator (with data from differential GPS, sun detector, magnetometer?)

DMM-32DX-AT board

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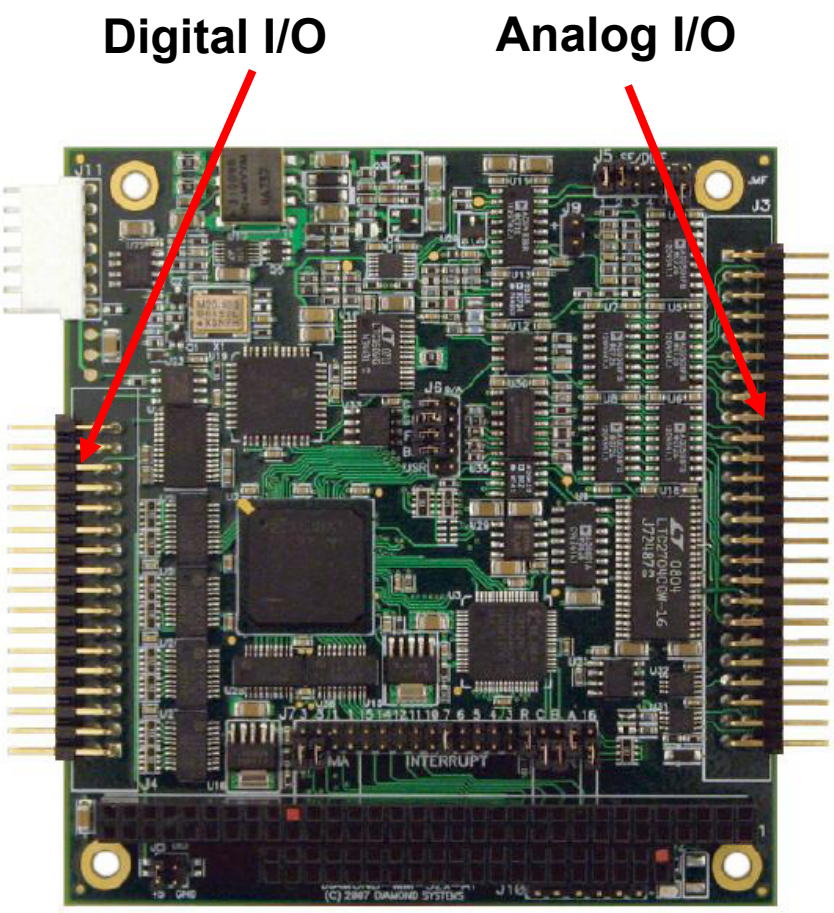

Digital Input/Output

- 24 Digital lines configurable as input or output in banks of 8
- Serial port

Analog Input/Output

- 32 single ended / 16 differential 16-bit ADC, multiple ranges
- 4 16-bit DAC outputs

FIFO

1024-sample FIFO available if needed (probably not in our case)

DMM-32DX-AT

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- 2 DMM-32DX-AT boards needed for pGAPS
- Hardware address is jumper selectable
- Board 1
  - 32 single ended inputs
    - temperatures
- Board 2
  - 16 differential inputs
    - Current transducers
    - Pressure transducers
    - Magnetometer readings
  - 2 analog outputs
    - rotator torque
    - pump speed

I/O connectors

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J3: Analog I/O Header

AGND	1	2	AGND
Vin 0 / 0+	3	4	Vin 16 / 0-
Vin 1 / 1+	5	6	Vin 17 / 1-
Vin 2 / 2+	7	8	Vin 18 / 2-
Vin 3 / 3+	9	10	Vin 19 / 3-
Vin 4 / 4+	11	12	Vin 20 / 4-
Vin 5 / 5+	13	14	Vin 21 / 5-
Vin 6 / 6+	15	16	Vin 22 / 6-
Vin 7 / 7+	17	18	Vin 23 / 7-
Vin 8 / 8+	19	20	Vin 24 / 8-
Vin 9 / 9+	21	22	Vin 25 / 9-
Vin 10 / 10+	23	24	Vin 26 / 10-
Vin 11 / 11+	25	26	Vin 27 / 11-
Vin 12 / 12+	27	28	Vin 28 / 12-
Vin 13 / 13+	29	30	Vin 29 / 13-
Vin 14 / 14+	31	32	Vin 30 / 14-
Vin 15 / 15+	33	34	Vin 31 / 15-
Vout 3	35	36	Vout 2
Vout 1	37	38	Vout 0
Vref Out	39	40	Agnd
A/D Convert	41	42	Ctr 2 Out / Dout 2
Dout 1	43	44	Ctr 0 Out / Dout 0
Extclk / Din 3	45	46	Extgate / Din 2
Gate 0 / Din 1	47	48	Clk 0 / Din 0
+5V	49	50	Dgnd

J4: Digital I/O Header

A7	1	2	A6
A5	3	4	A4
A3	5	6	A2
A1	7	8	A0
B7	9	10	B6
B5	11	12	B4
B3	13	14	B2
B1	15	16	B0
C7	17	18	C6
C5	19	20	C4
C3	21	22	C2
C1	23	24	C0
Latch	25	26	Ack
NC	27	28	NC
(RS-232) Tx	29	30	Rx (RS-232)
(RS-485) Rx/Tx +	31	32	Rx/Tx - (RS-485)
+5V	33	34	Dgnd

Analog output configuration

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A

Agnd	1	2	Agnd
0	3	4	16
1	5	6	17
2	7	8	18
3	9	10	19
4	11	12	20
5	13	14	21
6	15	16	22
7	17	18	23
8	19	20	24
9	21	22	25
10	23	24	26
11	25	26	27
12	27	28	28
13	29	30	29
14	31	32	30
15	33	34	31
	35-50 Same as p. 7		

B

Agnd	1	2	Agnd
0+	3	4	0-
1+	5	6	1-
2+	7	8	2-
3+	9	10	3-
4+	11	12	4-
5+	13	14	5-
6+	15	16	6-
7+	17	18	7-
8+	19	20	8-
9+	21	22	9-
10+	23	24	10-
11+	25	26	11-
12+	27	28	12-
13+	29	30	13-
14+	31	32	14-
15+	33	34	15-
	35-50 Same as p. 7		

C

Agnd	1	2	Agnd
0+	3	4	0-
1+	5	6	1-
2+	7	8	2-
3+	9	10	3-
4+	11	12	4-
5+	13	14	5-
6+	15	16	6-
7+	17	18	7-
8	19	20	24
9	21	22	25
10	23	24	26
11	25	26	27
12	27	28	28
13	29	30	29
14	31	32	30
15	33	34	31
	35-50 Same as p. 7		

D

Agnd	1	2	Agnd
0	3	4	16
1	5	6	17
2	7	8	18
3	9	10	19
4	11	12	20
5	13	14	21
6	15	16	22
7	17	18	23
8+	19	20	8-
9+	21	22	9-
10+	23	24	10-
11+	25	26	11-
12+	27	28	12-
13+	29	30	13-
14+	31	32	14-
15+	33	34	15-
	35-50 Same as p. 7		

Analog output configuration is jumper selectable. The most suitable configuration is still TBD, but it should be possible to know in a few weeks.

Housekeeping wiring

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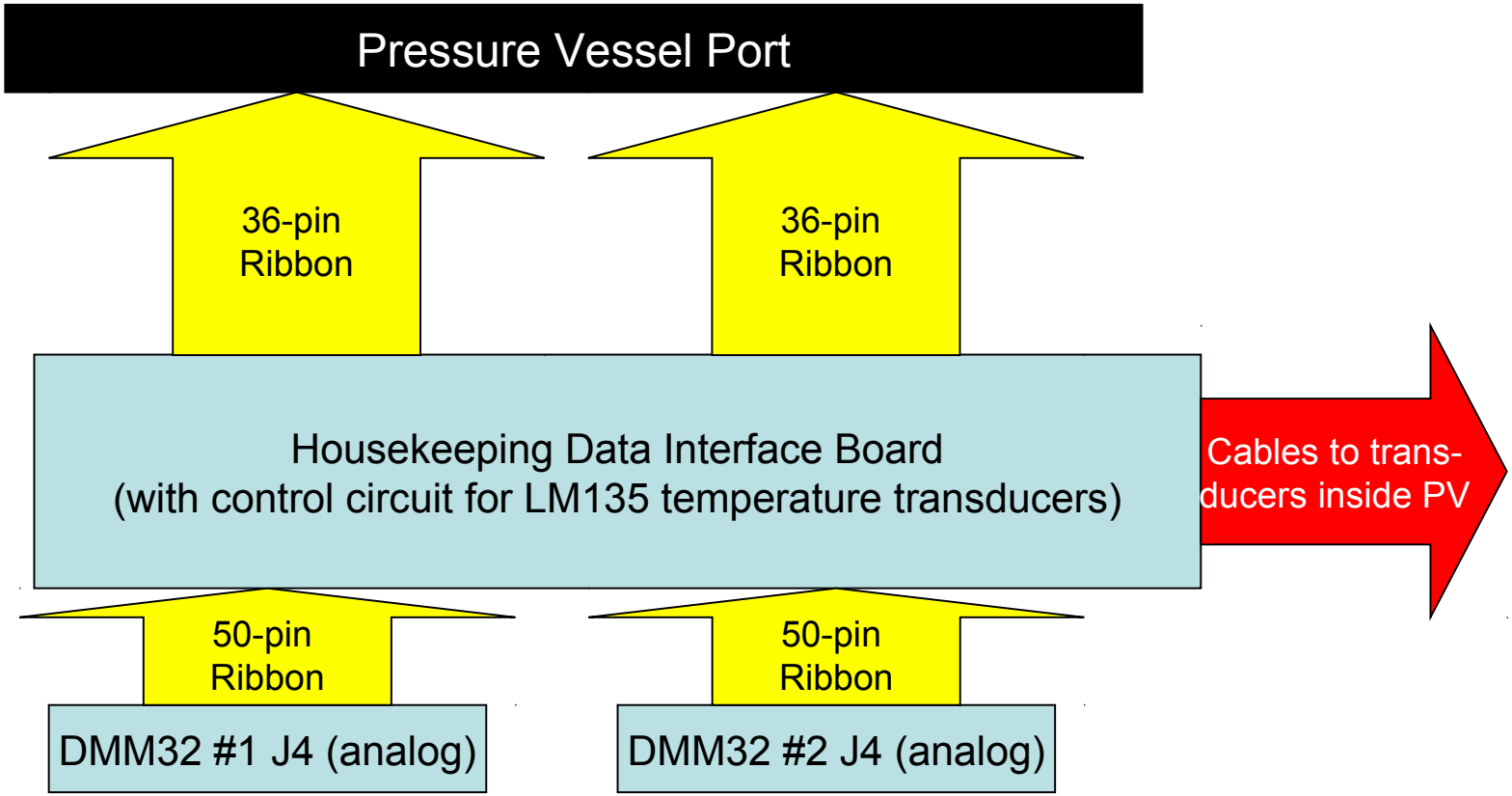

Some kind of interface board will be needed to bring the 50-pin Ribbon cable from the DMM32 Analog Connector to the 36-pin feedthroughs on the pressure vessel. In addition, most housekeeping signals will come from outside the pressure vessel, but some will come from inside the pressure vessel. One solution could be an interface board that provides the bias voltages for the LM135 temperature transducers and also merges signals from inside and outside the pressure vessel. This idea is still preliminary.

Feedthrough for analog signals

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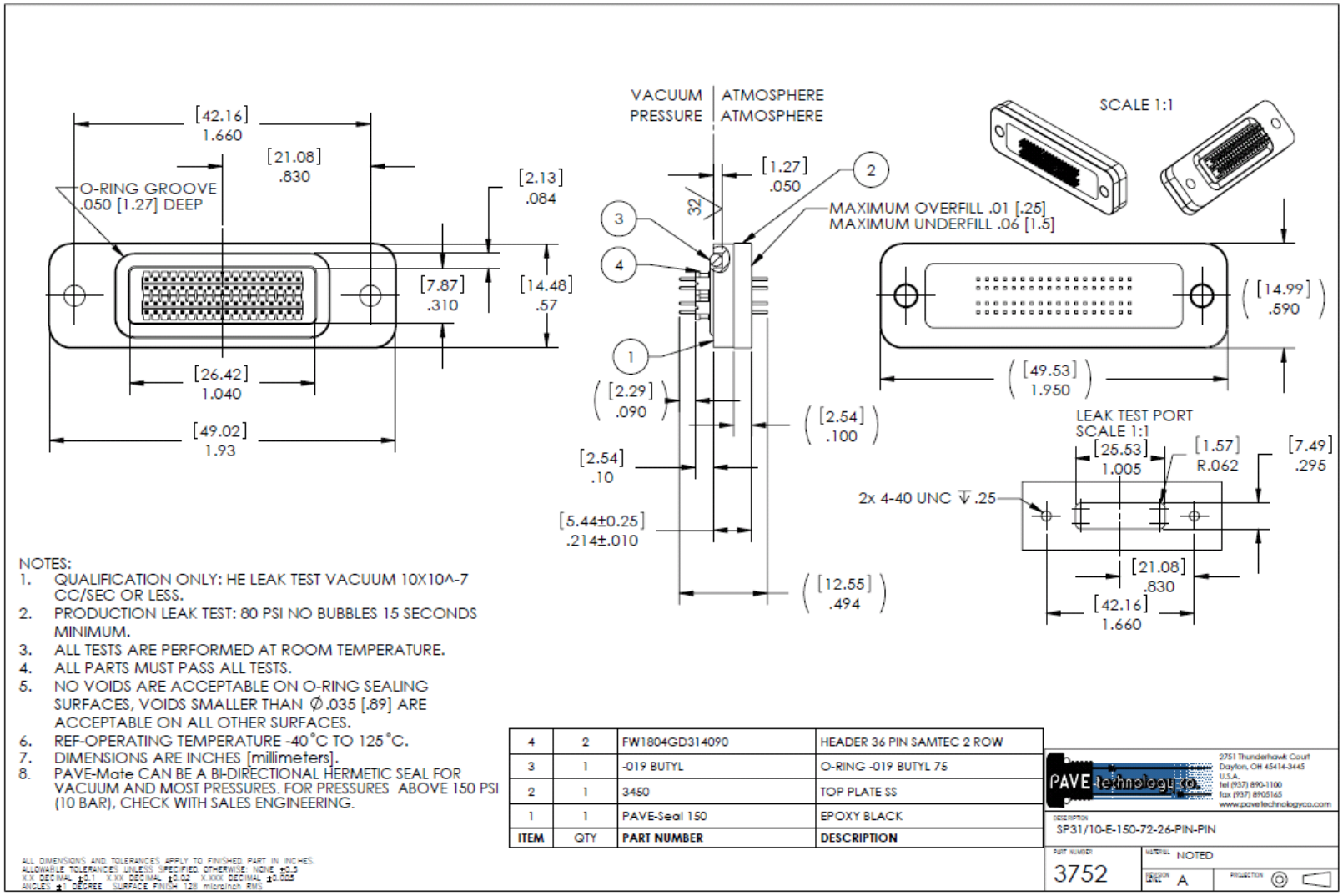

NOTES:
1. QUALIFICATION ONLY: HE LEAK TEST VACUUM 10X10^-7 CC/SEC OR LESS.
2. PRODUCTION LEAK TEST: 80 PSI NO BUBBLES 15 SECONDS MINIMUM.
3. ALL TESTS ARE PERFORMED AT ROOM TEMPERATURE.
4. ALL PARTS MUST PASS ALL TESTS.
5. NO VOIDS ARE ACCEPTABLE ON O-RING SEALING SURFACES, VOIDS SMALLER THAN Ø.035 [.89] ARE ACCEPTABLE ON ALL OTHER SURFACES.
6. REF-OPERATING TEMPERATURE -40°C TO 125°C.
7. DIMENSIONS ARE INCHES [millimeters].
8. PAVE-Mate CAN BE A BI-DIRECTIONAL HERMETIC SEAL FOR VACUUM AND MOST PRESSURES. FOR PRESSURES ABOVE 150 PSI (10 BAR), CHECK WITH SALES ENGINEERING.

ITEM	QTY	PART NUMBER	DESCRIPTION
4	2	FW1804GD314090	HEADER 36 PIN SAMTEC 2 ROW
3	1	-019 BUTYL	O-RING -019 BUTYL 75
2	1	3450	TOP PLATE SS
1	1	PAVE-Seal 150	EPOXY BLACK

PAVE technology co.
2751 Thunderhawk Court
Dayton, OH 45414-3445
U.S.A.
tel (937) 890-1100
fax (937) 890-5165
www.pavetechnologyco.com

DESCRIPTION: SP31/10-E-150-72-26-PIN-PIN
PART NUMBER: 3752
MATERIAL: NOTED
REVISION: A

ALL DIMENSIONS AND TOLERANCES APPLY TO FINISHED PART IN INCHES
ALLOWABLE TOLERANCES UNLESS SPECIFIED OTHERWISE: NONE ±0.5
X.X DECIMAL ±0.1 X.XX DECIMAL ±0.02 X.XXX DECIMAL ±0.005
ANGLES ±1° DEGREE SURFACE FINISH 128 microinch RMS

Housekeeping

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- Send housekeeping event to flight computer every 60 seconds
- Readout transducers every second to obtain averages
- Readout by polling the board from the flight computer. (The board can be configured to generate interrupts, but this functionality seems unnecessary.)

Housekeeping signals

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Single Ended 0—10V (24):

1. Internal ambient temperature inside the gondola (on a copper slug for air temp)
2. Internal wall surface temperature of gondola
3. Internal vessel air temperature (TOF Vessel)
4. Vessel end plate temperature (TOF Vessel)
5. Vessel end plate temperature (UCB vessel)
6. Vessel end plate temperature (detector vessel)
7. Radiator temperature
8. Fluid loop temperature 1
9. Fluid loop temperature 2
10. Si(Li) detector temperature 1
11. Si(Li) detector temperature 2
12. Si(Li) detector temperature 3
13. Temperature sensor (TBD)
14. Temperature sensor (TBD)
15. Temperature sensor (TBD)
16. Temperature sensor (TBD)
17. UCB DAQ current (Relay 0)
18. TOF system current: all but +5V (Relay 1)
19. TOF system current: +5V converter (Relay 2)
20. Flight CPU/GPS current (Relay 3)
21. Fluid loop pump current (Relay 4)
22. Rotator current (Relay 5)
23. X-ray tube current (Relay 6)

Differential

1. Pressure Vessel pressure transducer
2. Water-tight vessel pressure transducer
3. External pressure transducer
4. Si(Li) HV readback
5. Magnetometer Bx (TBD)
6. Magnetometer By (TBD)
7. Magnetometer Bz (TBD)
8. Sun sensor (TBD)
9. Static Pressure Sensor 1 (for cooling fluid)
10. Static Pressure Sensor 2 (for cooling fluid)

- read also temperatures from TOF?
- how are currents and voltages electrically isolated from the flight computer?
- read voltage from power supplies with reference voltage?

Clock board

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- Synchronizes all subsystem clocks so events have the same time tag
- 10 MHz clock provides 100ns resolution
- 32 bit counter
- Clock and sync signal generated in the flight computer
- Isolated signals maintain ground isolation
- Implemented with discrete logic or in FPGA
- Functional Operation
  - Clock value to be loaded sent to all subsystems over the network
  - After appropriate delay a synchronous load signal causes all subsystem counters to be loaded with this value in a single clock time

Clock signals

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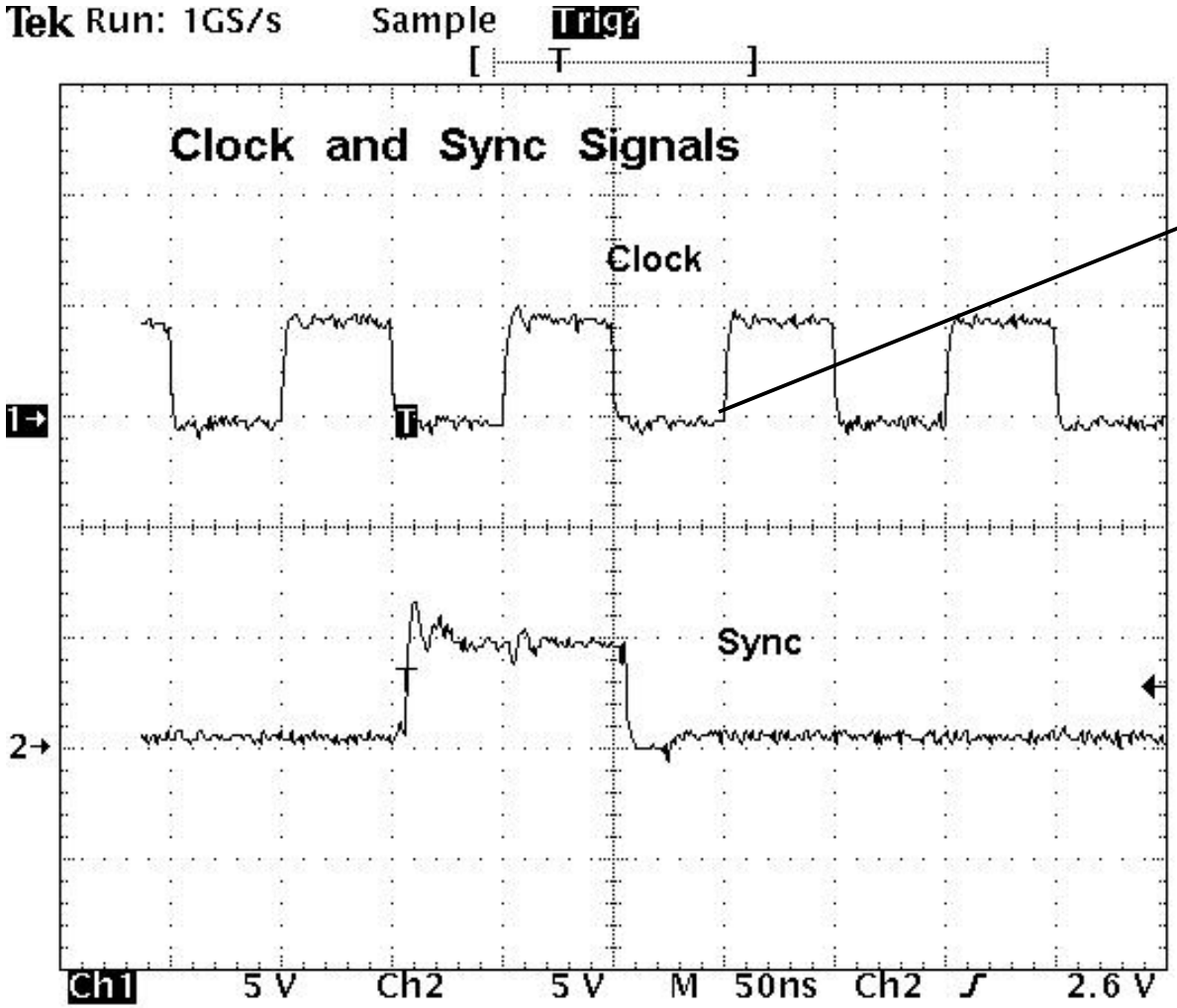

increment on rising edge

Simplified schematic

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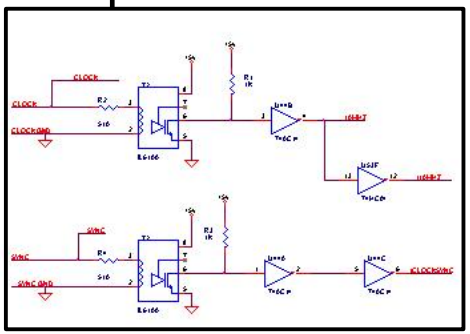
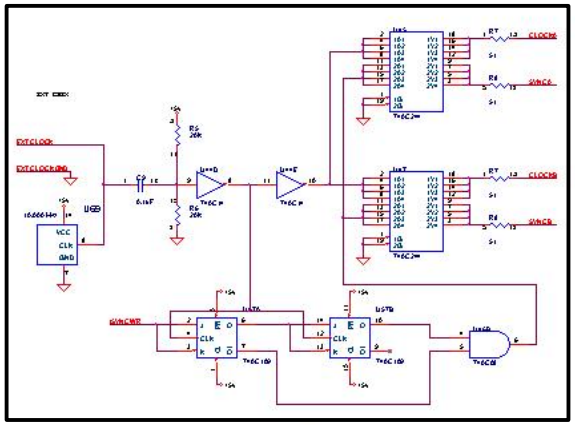
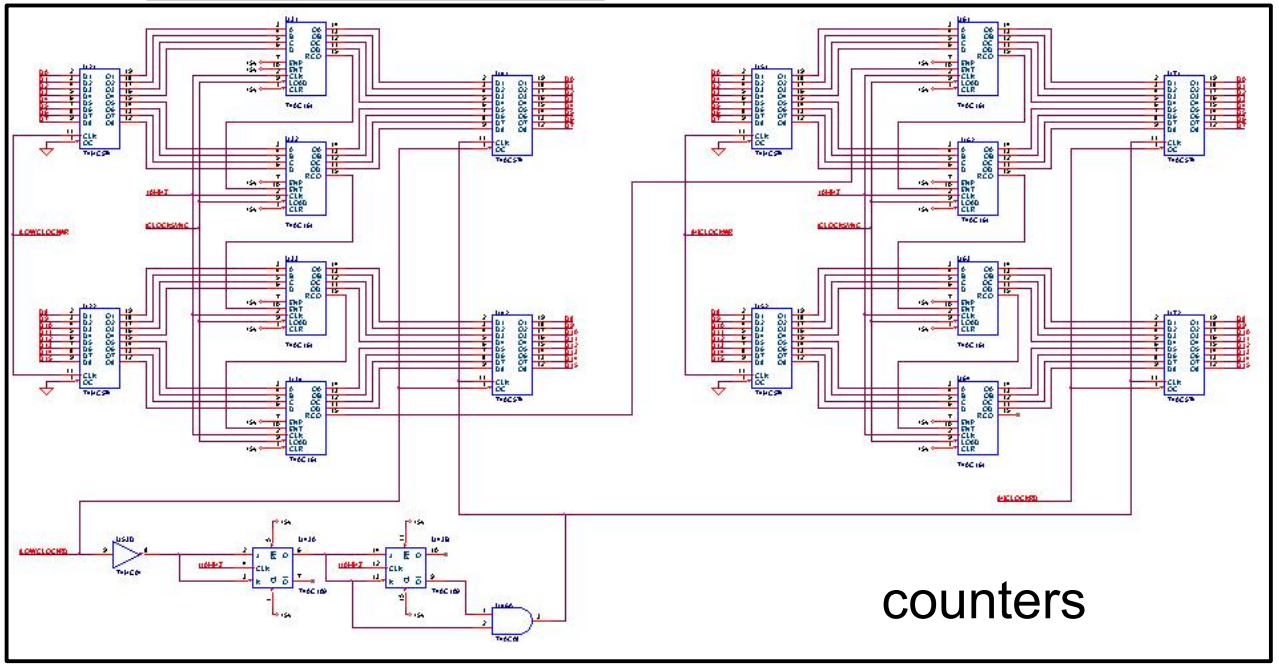
- TOF should electrically isolate clock signal
- UCB will electrically isolate busy/trigger signals for UCLA

input isolators





clock generator



counters

Housing

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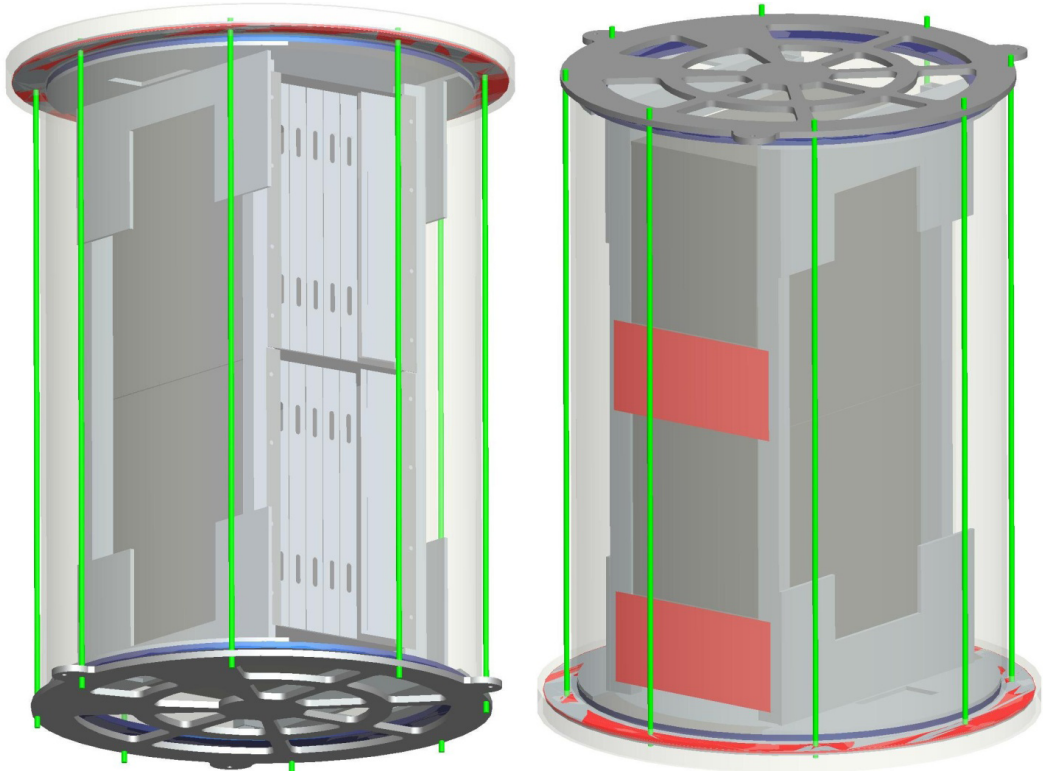

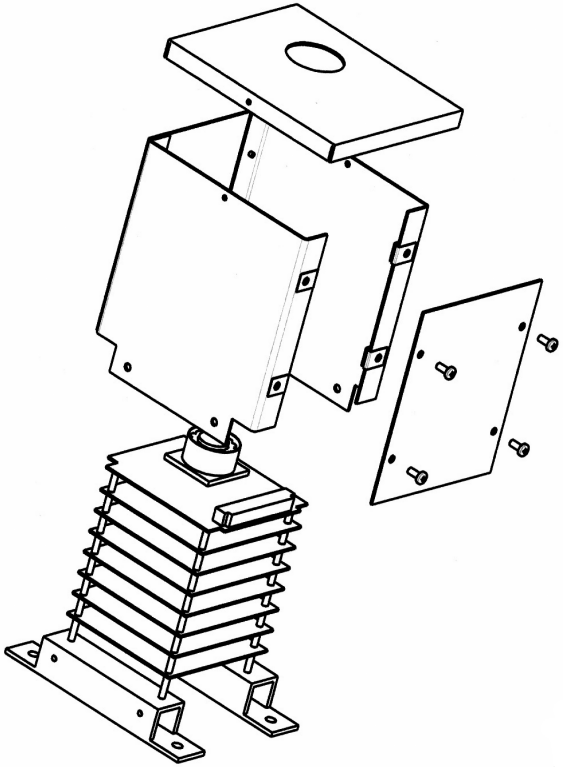

- unpressurized card cage vessel: breather/vent in air, swells after contact with water
- how to access card cages: flexible conduit? cable slacks?
- heat sink: CCs are mounted on rails and vessel end plates are radiators, needs verification

- flight computer will be placed in TOF pressure vessel
- flight computer housing

Flight computer software

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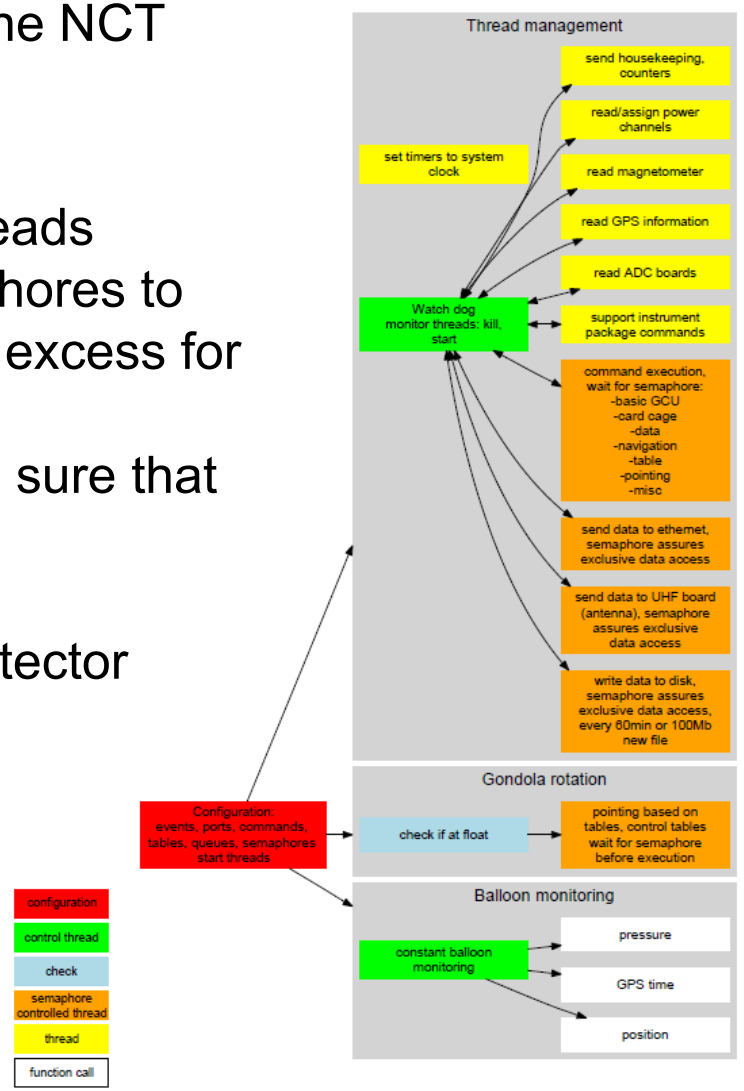
- flight computer software design is based on the NCT software written in C
- program is based on the usage of pthreads:
  - watchdog thread controls some of the threads
  - some threads rely on the usage of semaphores to assure safe execution e.g. exclusive data excess for writing/sending, commanding
- commands for gondola rotation have to make sure that the radiator is pointed away from the sun
- Flight housekeeping (attitude, GPS)
- Ethernet communication uses UDP for subdetector communication
- interface to telemetry via serial connection
- clock board sends time to subdetectors
- working flight code framework until 11/12/10 (will need more coding for DIO commands, TOF, Si(Li), rotator, HK, GPS, serial as we move on)



Commands

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Digital Commands:

1. Relay 0 (UCB Card Cages, pre-amps, detector HV)
2. Relay 1 (TOF +/-12 V power converter)
3. Relay 2 (TOF +5V power converter)
4. Relay 3 (Flight CPU power supply module, needs to be special command, **LAST command**)
5. Relay 4 (Fluid Loop System)
6. Relay 5 (Rotator)
7. Relay 6 (X-ray source)
8. Relay 8 (Spare)
9. Relay 9 (Spare)

Analog Commands:

1. Rotator: 1 DAC level to set torque level
2. Fluid loop pump: 1 DAC level to set flow rate (check with Gordon)

Flight computer commands

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- power on/off instruments
- restart/reset DSP
- default configuration
- set voltages
- set thresholds
- set trigger mode (TOF, self-trigger)
- synchronize time
- read data
- read counter
- read livetime
- read flight housekeeping
- read disk status
- read error status
- rotator commands
- relay control for all instruments
- cooling pump speed

Ground computer

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Ground computer is connected to ISAS using RS232

- data will be distributed to a few different computers
- main computer computer controls commands to be send the balloon

Software - two options:

- NCT ground computer software exists and could be modified for pGAPS based on C
- new software using QT

Needed functionalities:

- all commands implemented in the flight software must be executable from the ground computer
- data display: spectra of raw, calibration and TOF heartbeat data
- event display: basic track fits
- monitoring of detector status: livetime, temperatures, currents, GPS position
- other diagnostic display

schedule: working framework: 2/4/11

Software testing

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- using mock data streams to simulate the different subsystems (based on Geant Monte Carlo)
- sending out data to RS232 to simulate JAXA telemetry and format for packing
- display data in ground computer software and send commands
- use test signals as well as real Si(Li) signals

- test functionalities of power distribution board
- test functionalities of DMM32 board with Florian
- work with UCLA on the TOF format

JAXA format

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Uplink

RS232C (Serial):

start bit + BALID (command type, 4 bits) + VCID (multi-user), 4 bits)

+ stop bit (2 bits)

+ start bit

+ data (1byte)

+ stop bit (2bits)

+ start bit

+ CKC-CCITT (1 byte)

+ stop bit (2 bits)

+ start bit

+ CKC-CCITT (1 byte)

+ stop bit (2 bits)

1 byte of user data with max. 54.5bps → max. transmission of ~13KB data during 3h flight time (~every 3s one 10B command)

AVOID LONG COMMANDS

Downlink

Frame: 256 bytes fixed

1-2 Sync Code

3-6 Frame Counter

7 BALID/VCID

8 VC Counter

9 length

10 surplus byte

11-254 user data

255-256 Error Correction

244 byte of user data with max. 57.8kbps → max. transmission of ~75MB data during 3h flight time

TOF and Si(Li) data

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- **TOF** (only estimates, needs more input from TOF group)
  - **raw** data size per event: 20B header + 36 PMT information (2B ADC, 2B time): **164B**
  - **zero-suppressed** data size per event: 20B header + only non-zero PMT information (2B ADC, 2B time):
    3 TOF trigger: 64B
    2 TOF trigger: 56B
- **Si(Li):**
  - **zero-suppressed** data size per event: 20B header + only non-zero Si(Li) information (2B low or high gain ADC per hit)

Monitoring data size

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Type:	Size/Trigger [Byte]	Rate [Hz]	Size [Mbyte]
TOF Housekeeping	100	1	1.08
TOF Counter	150	1	1.62
TOF Lifetime	8	1	0.09
Tracker Housekeeping	86	1	0.93
Tracker Counter	72	1	0.78
Tracker Lifetime	8	1	0.09
Settings: temperatures, currents, balloon info	70	0.02	0.02
GPS	30	1	0.32
Calibration assuming burst mode calibration (1min with 1KHz every 30min)	22	33.33	7.92
Heart beat, raw all channels of TOF and Tracker	164	1	1.77
Command copy			0.02
			14.62

continuous data readout of status information

byte	7	6	5	4	3	2	1	0
0	packet type = 8				DSP ID			
1	board ID							
2	system clock: bit 0-7							
3	system clock: bit 8-15							
4	system clock: bit 16-23							
5	system clock: bit 24-31							
6-20	AD converter							
21	active boards mask: $1F$ =all 5 boards active							
22	control: bit 0-7							
23	control: bit 8-15							
24	fast enabled: bit 0-7							
25	fast enabled: bit 8-15							
26	slow enabled: bit 0-7							
27	slow enabled: bit 8-15							
28	system clock MSB: bit 0-7							
29	system clock MSB: bit 8-15							
30	system clock LSB: bit 0-7							
31	system clock LSB: bit 8-15							
32	fast window: bit 0-7							
33	fast window: bit 8-15							
34	slow time: bit 0-7							
35	slow time: bit 8-15							
36	slow window: bit 0-7							
37	slow window: bit 8-15							
38	shield time: bit 0-7							
39	shield time: bit 8-15							
40	guard time: bit 0-7							
41	guard time: bit 8-15							
42-49	DAC 0 threshold settings							
50-57	DAC 1 threshold settings							
58-65	DAC 2 threshold settings							
66-73	DAC 3 threshold settings							
74	guard window: bit 0-7							
75	guard window: bit 8-15							
76	convert time: bit 0-7							
77	convert time: bit 8-15							
78	tthresh							
79	error type[1]							
80	error count: bit 0-7							
81	error count: bit 8-15							
82	DSP 2: bit 0-7							
83	DSP 2: bit 8-15							
84	DSP 3: bit 0-7							
85	DSP 3: bit 8-15							

existing NCT format, must be adapted to the new ACTEL logic

Si(Li) – Livetime & counter format

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livetime

byte	7	6	5	4	3	2	1	0
0	packet type = 6				DSP ID			
1	livetime: bit 0-7							
2	livetime: bit 8-15							
3	livetime: bit 16-23							
4	system clock: bit 0-7							
5	system clock: bit 8-15							
6	system clock: bit 16-23							
7	system clock: bit 24-31							

counter

byte	7	6	5	4	3	2	1	0
0	packet type = 2				DSP ID			
1	board ID							
2	system clock: bit 0-7							
3	system clock: bit 8-15							
4	system clock: bit 16-23							
5	system clock: bit 24-31							
$6+2\cdot i, i=0\ldots15$	low level discriminator for each ch. i: bit 0-7							
$7+2\cdot i, i=0\ldots15$	low level discriminator for each ch. i: bit 8-15							
$38+2\cdot i, i=0\ldots15$	upper level discriminator for each ch. i: bit 0-7							
$39+2\cdot i, i=0\ldots15$	upper level discriminator for each ch. i: bit 8-15							
69+70 [71+72	TOF triggered self-triggered]							

Trigger modes – 3 TOF planes

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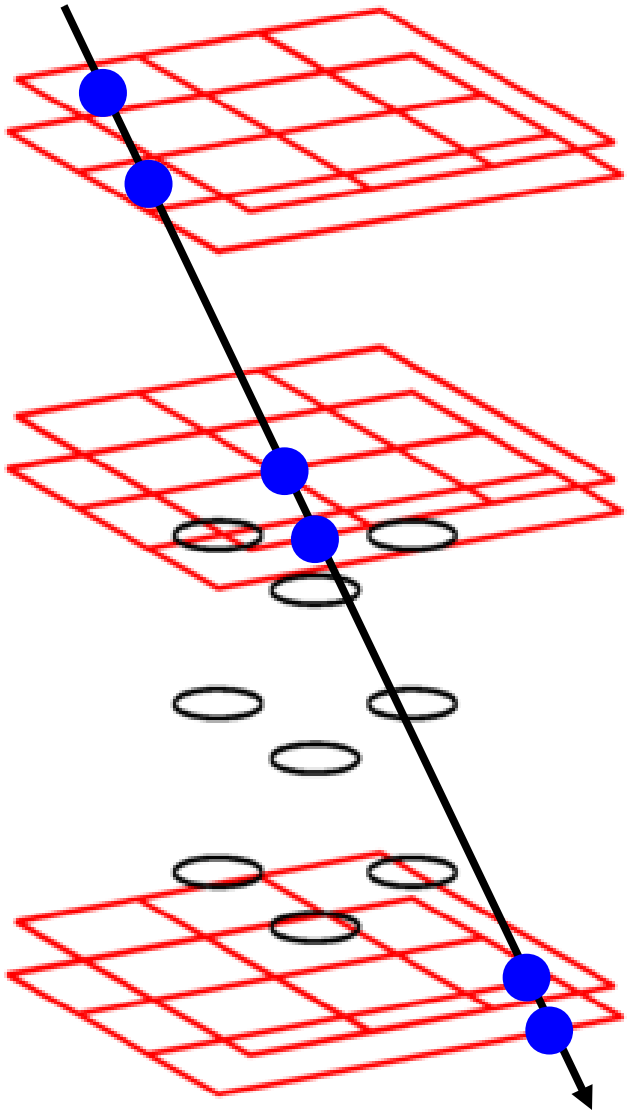
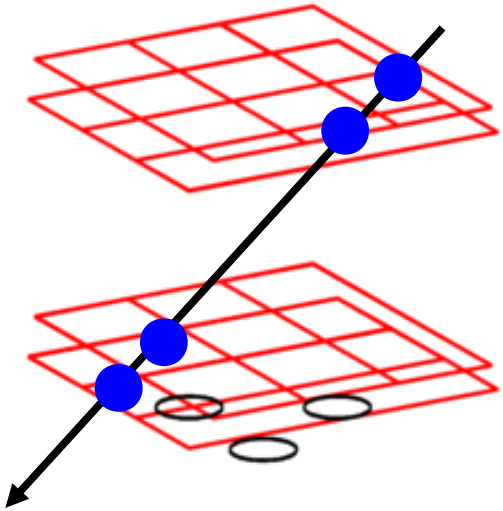


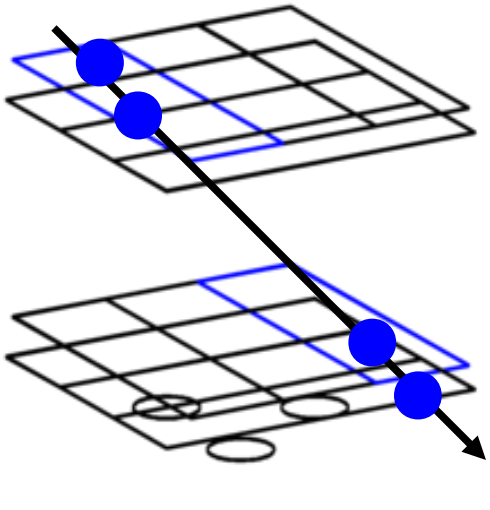
- all 3 TOF planes fired (always require 1 hit in x and 1 in y direction)
- data size:
  - **28Hz:**
    raw: 69MB - 6.4KB/s
    (TOF: 70%, TRK: 9%)
    comp: 41MB - 3.8KB/s
    (TOF: 49%, TRK: 16%)

Trigger modes – 2 TOF planes

pGAPS



2 TOF trigger

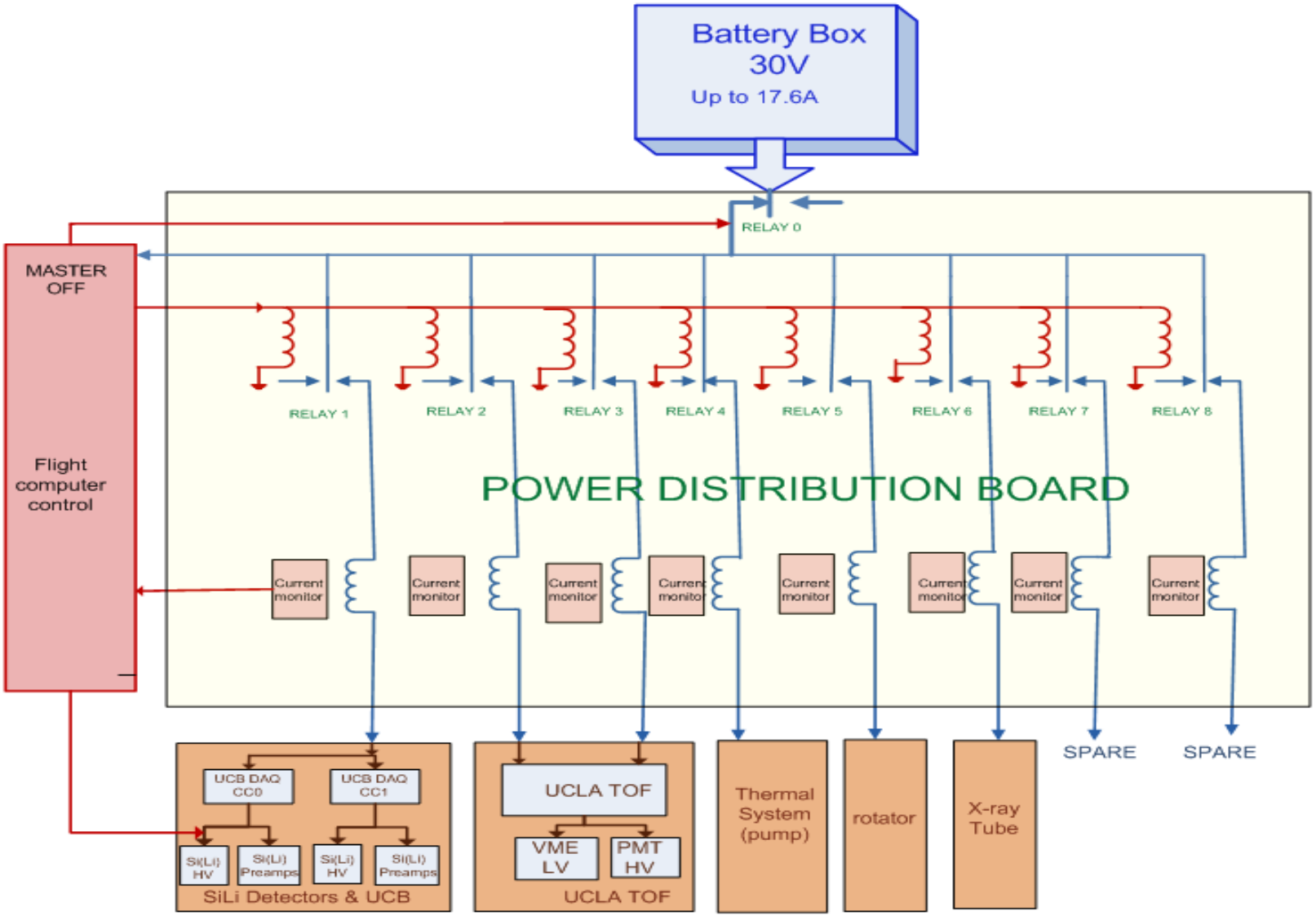


veto all highly inclined TOF events (and also other 3 combinations)

- upper and middle TOF planes fired
- If data size too large, maintain possibility to prescale events
- data size:
  - **no veto (121Hz): comp:** 114MB - 10.6KB/s (TOF: 64%, TRK: 24%)
  - **veto (88Hz): comp:** 88MB - 8.1KB/s (TOF: 61%, TRK: 23%)

Power distribution box block diagram

pGAPS



Power distribution box

pGAPS

TASKS AND SCHEDULE

	Task	Completion date
1	Determine current monitors	11/15/2010
2	Relay selection	11/15/2010
3	Finalize schematic, BB testing	11/30/2010
4	Order parts	12/3/2010
5	Assembly	1/20/2010
6	Testing	1/25//2010

Harnessing table

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Signal Name	From	To
+28V In	Power Distribution Box	UCB Card Cage
+28 RET	Power Distribution Box	UCB Card Cage
Preamp signals Det 0 X8	Si(Li) Det 0	UCB Card Cage
Preamp Power Det 0 +5V	UCB Card Cage	Preamp 0
Preamp Power Det 0 GND	UCB Card Cage	Preamp 0
Preamp Power Det 0 -5V	UCB Card Cage	Preamp 0
Preamp signals Det 8 X8	Si(Li) Det 8	UCB Card Cage
Preamp Power Det 8 +5V	UCB Card Cage	Preamp 0
Preamp Power Det 8 GND	UCB Card Cage	Preamp 0
Preamp Power Det 8 -5V	UCB Card Cage	Preamp 0
HV Power 0	UCB Card Cage	?
HV Power RET 0	UCB Card Cage	?
HV Power 1 ?	UCB Card Cage	?
HV Power RET 1?	UCB Card Cage	?
HV Power 2 ?	UCB Card Cage	?
HV Power RET 2?	UCB Card Cage	?
Ethernet 0	UCB Card Cage 0	Flight Computer
Ethernet 1	UCB Card Cage 1	Flight Computer
DSP reset 0	Flight Computer	UCB Card Cage 0
DSP reset 1	Flight Computer	UCB Card Cage 1
HV on_0	Flight Computer	UCB Card Cage
HV off 0	Flight Computer	UCB Card Cage
HV on_1	Flight Computer	UCB Card Cage
HV off_1	Flight Computer	UCB Card Cage
TOF trigger	TOF UCLA	UCB Card Cage
BUSY	UCB Card Cage	TOF UCLA
CLOCK	Flight Computer	UCB Card Cage
SYNC	Flight Computer	UCB Card Cage

TASKS AND SCHEDULE

	Task	Completion date	comment
1	Specify all connections	10/15/2010	
2	Specify all Connectors	10/22/2010	
3	Order parts	10/29/2010	
4	Mechanical drawing Back shells	10/26/2010	For Gore cables, custom shells
5	Delivery back shells	11/5/2010	
6	Test cables	11/9/2010	Start 11/1/2010
7	Flight cables	1/21/2010	

Power & mass

pGAPS

	Requirement		Present estimate	
Instrument component	Mass	Power	MASS	POWER
Preamp box		.30W/detector	1.8Kg all boxes	.30W/ detector
Card cage	20 Kg each	33W each	20 Kg each	33W each
Flight CPU	7 Kg	20W	1.5Kg	
Harnessing (to preamps)	15 Kg	0	1.5Kg	0
Other harnessing			*	
HV				
Signal Conditioning (Housekeeping)	1Kg	5W		
Power Conditioning (power distribution board)	3Kg		7 Kg	2W
UCB Vessel	71Kg	76W	31Kg (vessel only)	

*Need length

Summary of open issues

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1. Verify that signal conditioning (housekeeping) is not UCB responsibility. **[ok]**
2. Event Rates during self trigger mode, 30KHz? Above our event rate per strip. **[1-5KHz is maximum]**
3. Event rate, trigger mode **[must be less than 100Hz]**
4. Number of high voltages? How to connect them? Determine where to put them.
5. Grounding scheme HV, preamp power connector to Si(Li)
6. 3 more cables per card cage needed: HV on, HV off, DSP reset **[ok]**
7. When do the water proof containers go on. How do we do testing with potted cables through a hole? Is there an easy way to get to our cables inside?
8. Heat sinking of card cages **[ok]**
9. Harness length
10. Verify Mass estimates for UCB